

Modeling, Design and Implementation of High Gain Boost Converter with Voltage-mode Control for PV Systems

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Abstract- This paper presents modeling, design and implementation of a high gain boost DC-DC converter with voltage mode control for PV systems. Small signal model of the converter is developed from average state space analysis to obtain a control to output transfer function. A simple voltage mode analog controller is designed to regulate the output voltage of the converter. The operation of the converter under both steady state and transient state are validated experimentally. A hardware prototype of 50 Watt, 200V output voltage, 20kHz boost converter with an input of 12V is developed. The output voltage of dc-dc boost converter is regulated over a wide range of load variation (from 56% to 108% of full load).

Index Terms- voltage mode control, analog control, boost converter, PV systems.

I. INTRODUCTION

Photovoltaic (PV) source is most popular among sustainable power sources because of the availability of ample amount of solar energy. [1]. Many PV modules are connected together in series to increase their voltage and power capability for domestic and industrial applications. However, the maximum power of the PV system gets reduced due to mismatch of any PV source under different atmospheric conditions such as partial shading, ageing effects etc. There are several methods to extract the maximum power from a solar PV modules but they decrease the overall efficiency of the system. As photovoltaic (PV) source can have output of (12-48V) dc voltage. A high step-up dc-dc converter can boost the power and voltage for domestic and industrial applications. Therefore, it is better to connect a high step-up voltage gain dc-dc converter in a PV distributed system. A dc-dc converter connected with a PV distributed system is shown in Fig.1.

DC-DC Converters are of mainly classified under two categories isolate converters and non-isolated converters. Isolated converters like fly-back, forward, push-pull transformation ratio but it gives high voltage stress across switch and high power dissipation in leakage inductor [2]. To minimize the voltage spike across main switch, dissipative snubber (passive clamp) circuit or non-dissipative snubber (active clamp) circuit has been used at the cost of extra loss [3], [4].

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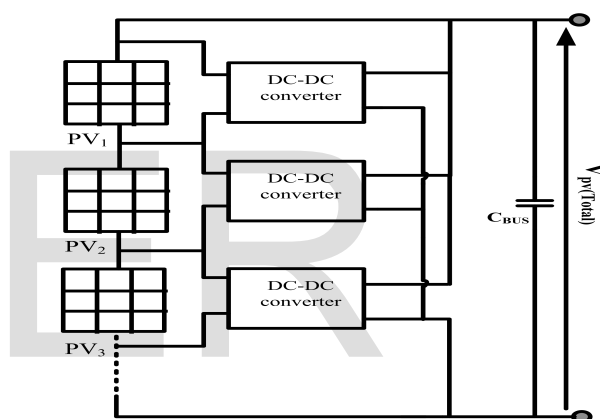


Fig. 1: Block diagram of dc-dc converters connected with a PV distributed system.

Non-isolated converters are used at high duty ratio to have high voltage gain but very high duty ratio results in high conduction loss in switch and also results a serious problem in diode reverse recovery [5], [6], [7].

There are different topologies to achieve high voltage gain some of them use switched capacitors technique and voltage lift techniques. These methods are capable of giving high voltage gain but with high transient current in switch and high conduction loss [8], [9], [10], [11].

The concept of coupled inductor was introduced in [12], [13], [14], [15], [16] to reduce the transients and voltage spikes across the semiconductor switches of the converter. For a distributed generation system from renewable sources like PV source, there is a need of front-end converters which should not only boost the output voltage of the PV source but also should regulate a constant voltage while inter facing with the inverter.

In [17] coupled inductor and voltage doubler technique is

used to get a high gain but this topology is acceptable for low output power and also occurs voltage ringing across power switch due to formation of tank circuit. There are topologies that have high conversion ratio used for PV application but with large no of component count [18]. High power output has been achieved by using coupled inductor [19], [20].

The PV current and voltage vary significantly by the variation in the atmospheric irradiance and temperature. The current generated by the series PV string is significantly limited by less illuminated PV modules in the string. The main factors responsible for non uniform illumination among PV modules in the string are partial shading, manufacturing defects, aging etc. Therefore, it becomes essential for dc-dc converter connected in PV string to regulate the output voltage under all uncertainties.

This paper presents design of a simple analog controller for the high gain boost converter with voltage mode control to regulate the output voltage for PV distributed systems. The circuit diagram of the converter is shown in Fig.2. [1].

Section II explains the principle of operation of the converter and develops the small signal model of the converter. Section III gives the proposed controller design. Section IV describes the design implementation and results. Section V concludes the work.

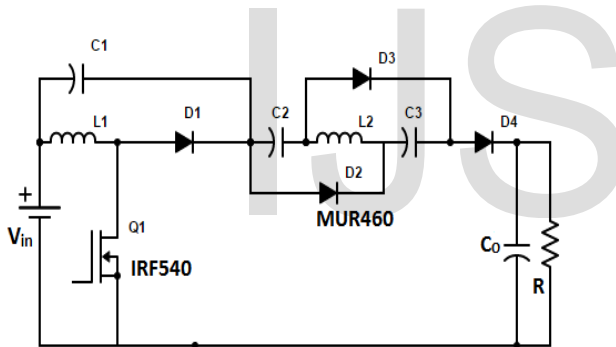


Fig. 2: Equivalent circuit diagram of the converter [1]

II. PRINCIPLE OF OPERATION AND SMALL SIGNAL MODELING

In this section the principle of operation of the converter is analyzed based on volt second balance and charge balance of inductor and capacitor over a switching time period respectively. Small signal modelling of the converter is developed based on state space analysis.

A. Principle of operation

There are six operating modes which are explained below.

1) *Mode I:* In this mode, switch Q_1 and diode D_4 are ON as shown in Fig.3(a). During this period, the inductor (L_1) charges. The current in primary winding increases linearly whereas current in secondary winding decreases linearly. Here output capacitor charges by series combination of dc source, clamp capacitor, intermediate capacitors and supplies energy to load R. This mode get completes at $t = t_1$ when current

in secondary winding equals to zero and starts to build in negative direction.

2) *Mode II:* In this mode, switch Q_1 , diodes D_2 and D_3 are ON as shown in Fig.3(b). Same as mode 1 input inductor increases and also transfers energy to the second inductor (L_2) by coupling. Current in secondary winding increases in negative direction. Therefore, diodes (D_2 and D_3) start conducting which starts charging of capacitors (C_2 and C_3) simultaneously. Output capacitor supplies load. This mode get completes at $t = t_2$ when switch turns off.

3) *Mode III:* In this mode, switch Q_1 turns OFF and diodes D_2 , D_3 are ON as shown in Fig.3(c). Energy from the primary winding of the inductor releases to parasitic capacitor of the switch C_{ds} . Some of the energy of primary winding of inductor charges capacitors (C_2 and C_3) simultaneously through secondary winding of inductor. This mode get completes at $t = t_3$, when switch capacitor is charged up to voltage equal to sum of supply voltage and voltage across clamp capacitor.

4) *Mode IV:* In this mode, switch Q_1 is OFF, diodes D_1 , D_2 , and D_3 are ON as shown in Fig.3(d). As the voltage across the parasitic capacitor (C_{ds}) goes more than the sum of dc source voltage and voltage across clamp capacitor, clamping diode D_1 gets forward biased and starts to conduct which provides path for energy of inductor to charge clamp capacitor and makes the voltage stress across switch constant. Same as previous mode some of the energy of primary of coupled inductor charges two capacitors simultaneously through diodes (D_2 and D_3) till secondary winding current equals to zero and output capacitor supplies energy to load R. This mode completes at $t = t_4$, when current in secondary winding equals to zero and diodes (D_2 and D_3) commutates.

5) *Mode V:* In this mode, switch Q_1 is OFF, diodes D_2 , and D_3 are ON as shown in Fig.3(e). the clamp capacitor (C_1) charges instantly. Energy stored in primary winding still supplies to clamp capacitor C_1 . As diodes D_2 D_3 have commutated so both capacitors (C_2 and C_3) supplies energy to output capacitor (C_o) and load R. This mode get completes at $t = t_5$, when clamp capacitor get fully charged and starts to discharge.

6) *Mode VI:* In this mode, switch Q_1 remains turn off as shown in Fig. 3(f). Input supply, clamp capacitor (C_1), two intermediate capacitors (C_2 and C_3) supplies energy in cascade to output capacitor and load R. This mode get completes at $t = t_6$, when positive gate pulse is given to switch to turn on for next cycle.

The key wave forms corresponding to above six modes of operation are shown in Fig.4. Out of these six modes, mode I, III, IV, V are of significantly less duration. Therefore, only mode II and VI are considered for steady state analysis.

During the mode II (for DT_S time duration) the voltage across inductor L_1 (V_{L1}) and the voltage across capacitor C_2 (V_{C2}) can be written as below.

$$V_{L1} = \frac{L_m + L_k}{L_m} V_{in} = k.V_{in} \quad (1)$$

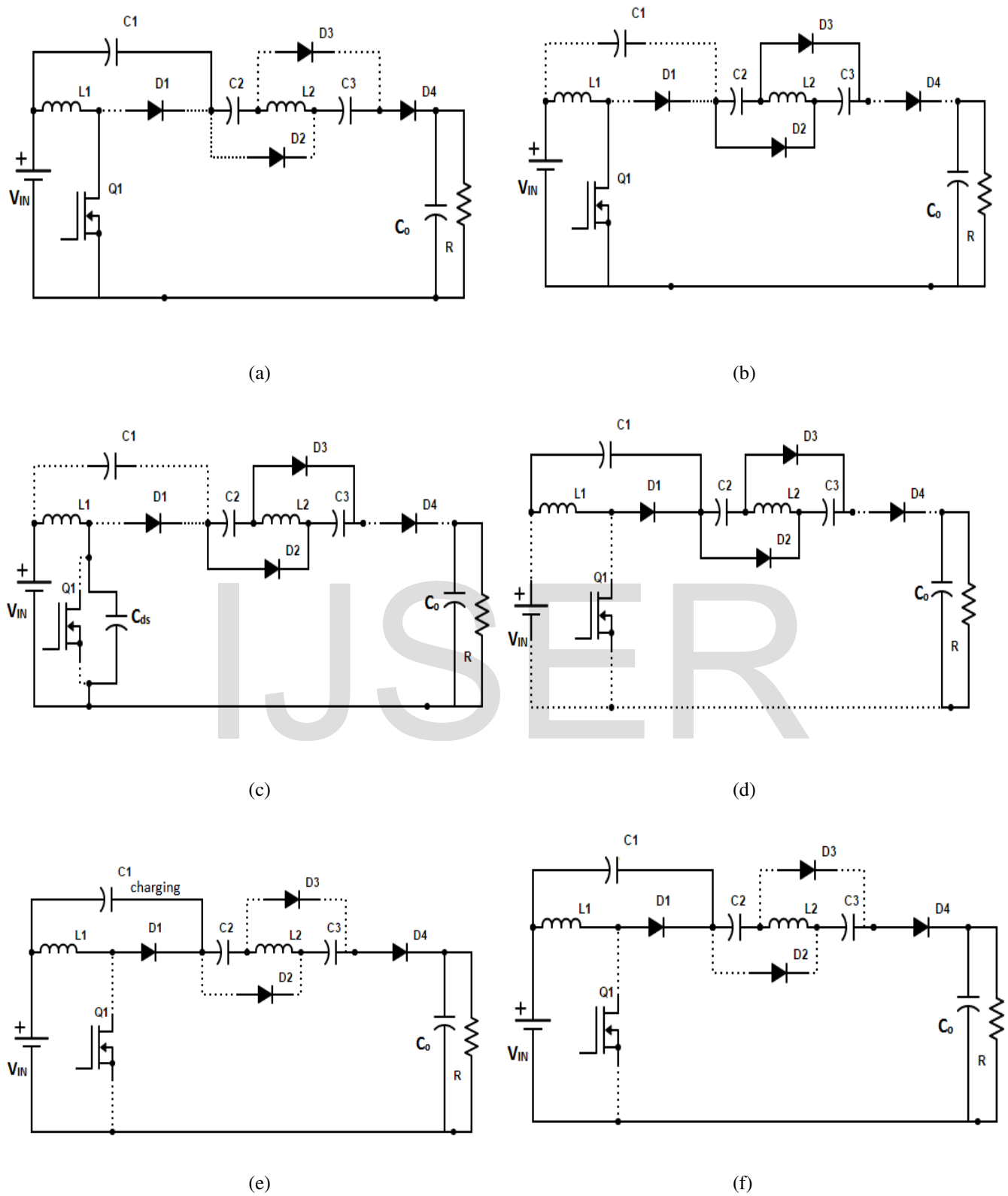


Fig. 3: Equivalent circuit diagram during each Operating modes in one switching period.(a) mode I. (b) mode II. (c) mode III. (d) mode IV. (e) mode V. (f) mode VI.

Where, L_m , L_k are the magnetizing and leakage inductance of inductor respectively. k is coefficient of coupling. n is secondary to primary turns ratio of the coupled inductor.

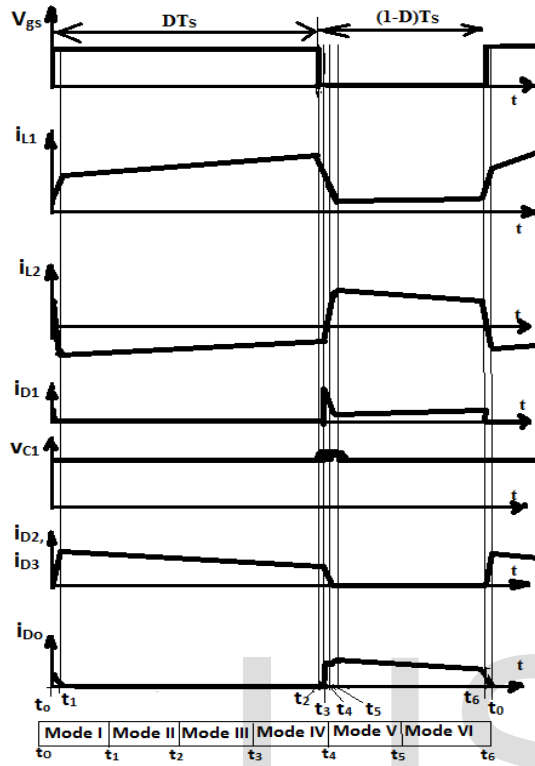


Fig. 4: Key wave forms corresponding to six modes of operation of the converter

During the mode VI (for $(1 - D)T_S$ time duration) the voltage across inductor L_1 (V_{L1}) and the voltage across capacitor C_1 (V_{C1}) can be written as below.

$$V_{C2} = V_{C3} = n.k.V_{in} \quad (2)$$

$$V_{L1} = V_{in} + V_{C1} + V_{C2} + V_{C3} - V_{C_o} \quad (3)$$

$$V_{C1} = \frac{D}{1-D} \cdot V_{in} \cdot \frac{(1+k) + (1-k).n}{2} \quad (4)$$

Using the principle of average voltage second balance of an inductor under continuous conduction mode (CCM) the expression of the voltage gain (M_{CCM}) is obtained as below.

$$M_{CCM} = \frac{1+n.k}{1-D} + n.k + \frac{D}{1-D} \cdot \frac{(1-k).(n-1)}{2} \quad (5)$$

The ideal voltage gain can be written as below for $k = 1$

$$M_{CCM} = \frac{1+n}{1-D} + n \quad (6)$$

The ideal voltage gain (M_{CCM}) under continuous conduction mode (CCM) v/s duty ratio (D) plot for different values of primary to secondary turns ratio (n) of the coupled inductor is as shown in Fig.5 below. It is observed from the plot that

converter can have highest possible gain of 16.67 at moderate duty ratio of (62%) when turns ratio (n) is equal to 4.

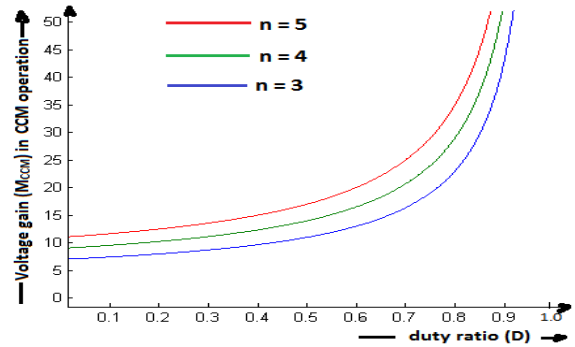


Fig. 5: Voltage gain (M_{CCM}) in CCM operation v/s duty ratio for different values of n.

B. Modeling of Converter

To study the transient behavior of the converter, the control to output transfer function of the converter is required. The control to output transfer function is derived by state space analysis of the converter under two significant modes of operation. These are mode II and Mode VI. The structure of equivalent circuits under mode II and VI are shown in Fig.6 and Fig.7 respectively.

1) Structure I: The equivalent circuit during the mode II of operation is as shown in Fig.6. The current through the inductor and the voltage across the capacitor are considered as state variable.

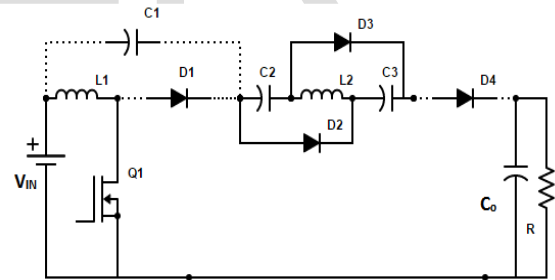


Fig. 6: Equivalent circuit diagram for structure I.

The state space equations for mode II are written as below.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L1} \quad (7)$$

$$\frac{di_{L2}}{dt} = \frac{v_{C2}}{L2} \quad (8)$$

$$\frac{dv_{C1}}{dt} = 0 \quad (9)$$

$$\frac{dv_{C2}}{dt} = \frac{dv_{C3}}{dt} = \frac{-0.5i_{L2}}{C2} \quad (10)$$

$$\frac{dv_{C_o}}{dt} = \frac{-v_{C_o}}{RC_o} \quad (11)$$

$$\dot{x} = A_1x + B_1u \quad (12)$$

$$\dot{y} = C_1x + D_1u \quad (13)$$

The state space equation for this mode in matrices form can be written as below.

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-0.5}{C_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$C_1 = [0 \ 0 \ 0 \ 0 \ 1]$$

2) *Structure II*: The equivalent circuit during the mode VI of operation is as shown in Fig.7. The current through the inductor and the voltage across the capacitor are considered as state variable.

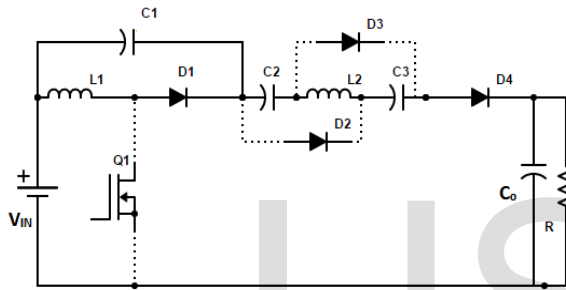


Fig. 7: Equivalent circuit diagram for structure II.

The state space equations for mode VI are written as below.

$$\frac{di_{L_1}}{dt} = \frac{-v_{C_1}}{L_1} \quad (14)$$

$$\frac{di_{L_2}}{dt} = \frac{V_{in} + v_{C_1} + 2v_{C_2} - v_{C_o}}{L_2} \quad (15)$$

$$\frac{dv_{C_1}}{dt} = \frac{i_{L_1} - i_{L_2}}{C_1} \quad (16)$$

$$\frac{dv_{C_2}}{dt} = \frac{dv_{C_3}}{dt} = \frac{-i_{L_2}}{C_2} \quad (17)$$

$$\frac{dv_{C_o}}{dt} = \frac{i_{L_2}}{C_o} - \frac{v_{C_o}}{RC_o} \quad (18)$$

$$\dot{x} = A_2x + B_2u \quad (19)$$

$$\dot{y} = C_2x + D_2u \quad (20)$$

The state space equations for this mode in matrices form can be written as below.

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{2}{L_2} & \frac{-1}{L_2} \\ \frac{1}{C_1} & \frac{-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix},$$

$$C_2 = [0 \ 0 \ 0 \ 0 \ 1]$$

The duration of mode II is dT_s and that of mode VI is $(1-d)T_s$. Therefore, state space equations for structure I and Structure II can be averaged and state space average model of the converter can be written as below. To find the small signal model of the converter, we linearize the model by perturbing every state variable about its steady state operating point.

$$\dot{x} = Ax + Bu \quad (21)$$

$$\dot{y} = Cx + Du \quad (22)$$

where

$$A = A_1d + A_2(1-d) \quad (23)$$

$$B = B_1d + B_2(1-d) \quad (24)$$

$$C = C_1d + C_2(1-d) \quad (25)$$

On substituting the values of $A_1, A_2, B_1, B_2, C_1, C_2$ in equations 24, 25, and 26, we find the average state space model of the converter which is given below.

$$A = \begin{bmatrix} 0 & 0 & \frac{(d-1)}{L_1} & 0 & 0 \\ 0 & 0 & \frac{1-d}{L_2} & \frac{2-d}{L_2} & \frac{d-1}{L_2} \\ \frac{1-d}{C_1} & \frac{d-1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{0.5d-1}{C_2} & 0 & 0 & 0 \\ 0 & \frac{1-d}{C_o} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{d}{L_1} \\ \frac{1-d}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix}, C = [0 \ 0 \ 0 \ 0 \ 1]$$

To find the small signal model of the converter, we linearize the model by perturbing every state variable about its steady state operating point.

$$i_{L_1} = I_{L_1} + \hat{i}_{L_1}, i_{L_2} = I_{L_2} + \hat{i}_{L_2}$$

$$v_{C_1} = V_{C_1} + \hat{v}_{C_1}, v_{C_2} = V_{C_2} + \hat{v}_{C_2}$$

$$v_{C_o} = V_{C_o} + \hat{v}_{C_o}, d = D + \hat{d}$$

Where, D is the duty ratio during steady state operation of the converter.

By substituting these perturbed values of state variables in average model, small signal model is derived as below.

$$\frac{di_{L_1}}{dt} = \frac{D-1}{L_1}v_{C_1} + \frac{V_{in} + V_{C_1}}{L_1}\hat{d} \quad (26)$$

$$\frac{di_{L_2}}{dt} = \frac{1-D}{L_2}v_{C_1} + \frac{2(1-D)}{L_2}v_{C_2} - \frac{1-D}{L_2}v_{C_o} + \frac{(n-1)V_{in} - V_{C_1} - 2V_{C_2} + V_{C_o}}{L_2}\hat{d} \quad (27)$$

$$\frac{dv_{C_1}}{dt} = \frac{(1-D)}{C_1}\hat{i}_{L_1} - \frac{(1-D)}{C_1}\hat{i}_{L_2} - \frac{I_{L_1} - I_{L_2}}{C_1}\hat{d} \quad (28)$$

$$\frac{dv_{C_2}}{dt} = \frac{(0.5D - 1)}{C_2} i_{L_2} + \frac{0.5I_{L_2}}{C_2} \hat{d} \quad (29)$$

$$\frac{dv_{C_o}}{dt} = \frac{(1 - D)}{C_o} i_{L_2} - \frac{1}{RC_o} v_{C_o} - \frac{I_{L_2}}{C_o} \hat{d} \quad (30)$$

Output equation can be written as below.

$$\hat{v}_o = v_{C_o} \quad (31)$$

On computing the state space model, the control to output voltage transfer function is calculated and written as below.

$$\frac{v_o \hat{s}}{d \hat{s}} = \frac{6250s^4 - 1.2e8s^3 + 8.14e10s^2 - 3.12e14s + 1.27e17}{s^5 + 12.5s^4 + 1.7e7s^3 + 2.07e8s^2 + 2.9e13s + 3.5e14} \quad (32)$$

The bode plot of Control to output transfer function of the converter is shown in Fig. 8.

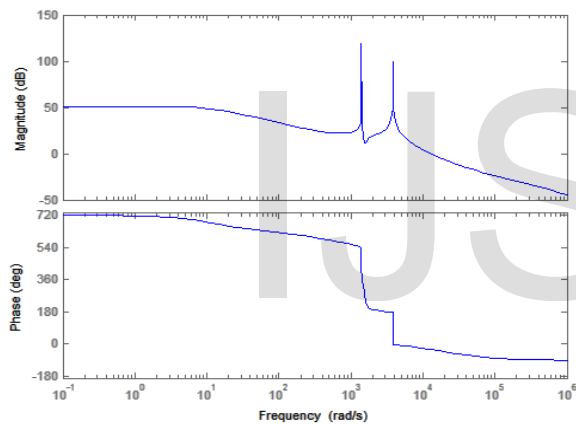


Fig. 8: Bode plot of control to output transfer function of the converter.

III. PROPOSED CONTROLLER DESIGN

The pole-zero map of the system transfer function is shown in Fig.10. It is observed from the pole-zero map of the converter that it provides sufficient phase to the system which ensures stability of the system. Therefore, it is not necessary to boost the phase of the system. In general TYPE II and TYPE III compensators are required if it is necessary to enhance the phase of the system by adding external phase shift [21]. Therefore, a simple TYPE I compensator is sufficient for the closed loop operation of the converter.

The proportional integral analog controller is designed as the TYPE I controller for the voltage mode control of the high step-up voltage gain dc-dc converter. The proportional gain (k_p) and integral gain (k_i) for the proportional-Integral (PI) controller are equal to 0.01 and 0.1 respectively. The block diagram of PI controller circuit diagram is shown in Fig. 9.

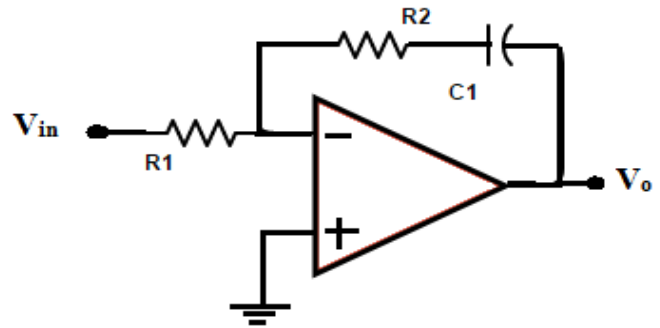


Fig. 9: The block diagram of PI controller circuit.

IV. DESIGN IMPLEMENTATION AND RESULTS ANALYSIS

A. Design specification

A 50Watt, 200V output voltage, 20 kHz high-step up voltage gain boost converter with 12V input voltage is designed with following specifications as shown in table 1 given below.

TABLE I: Design specification of the converter

Input voltage	12V
Output voltage	200V
Output power	50W
Switching frequency	20KHz
Duty ratio	62 %
Output voltage ripple	1%
Input current ripple	1%
Inductance of input inductor	243microH
Inductance of secondary inductor	3888 microH
Clamp capacitor	330microF
Intermediate capacitor	10microF
Output capacitor	100microF
MOSFET Switch	IRF540
DIODES	MUR460

The PI controller is implemented on the hardware by using the operational amplifier. The complete circuit of the high step-up gain dc-dc boost converter with proposed proportional-Integral (PI) controller is shown in Fig.11. The design of circuit is first carried out in pspice. Pspice simulation results are shown next.

B. Pspice Simulation Results

The open loop simulated results are shown as below. Fig.12 (a) and Fig.12 (b) show the key wave forms of voltage and current for inductors L_1 and L_2 respectively under continuous conduction mode (CCM). Fig. 12(c) shows the output voltage waveform under open loop operation of the converter. From Fig.12(d), it is noticed that voltage stress across switch has been clamped by using clamped capacitor (C_1) to sum of input voltage and voltage across clamped capacitor i.e. ($V_{in} + V_{C_1}$) which is equal to 30V.

Fig. 12(e) shows the output voltage of the converter when it is subjected to sudden and gradual change in load respectively. It is observed that converter is able to regulate the output voltage over a wide range of 56% to 108% of full load.

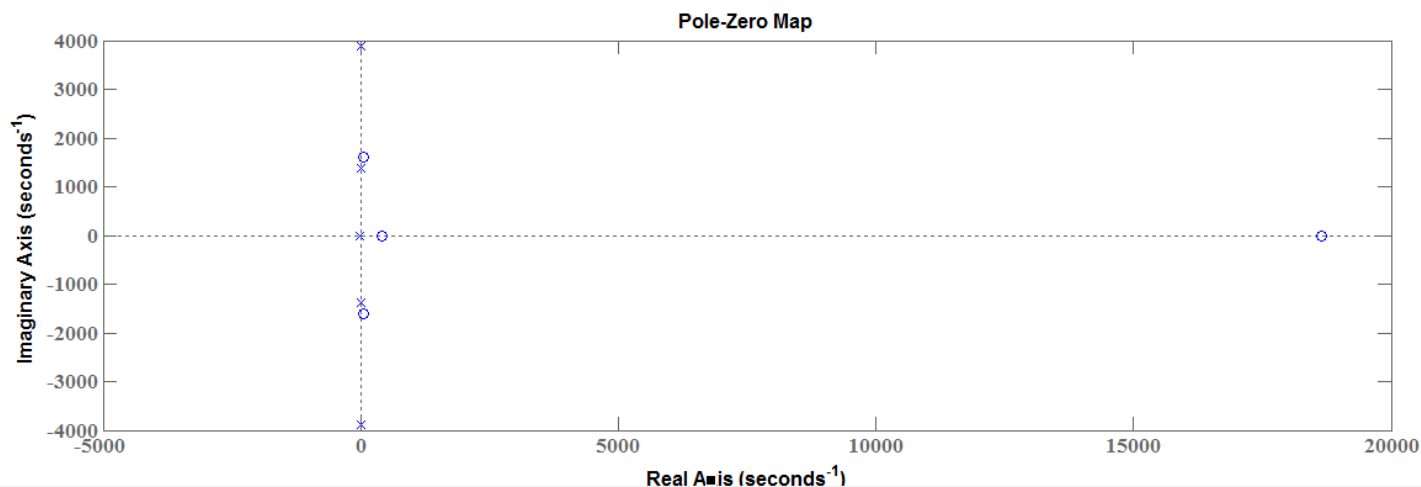


Fig. 10: pole-zero map of transfer function of the converter.

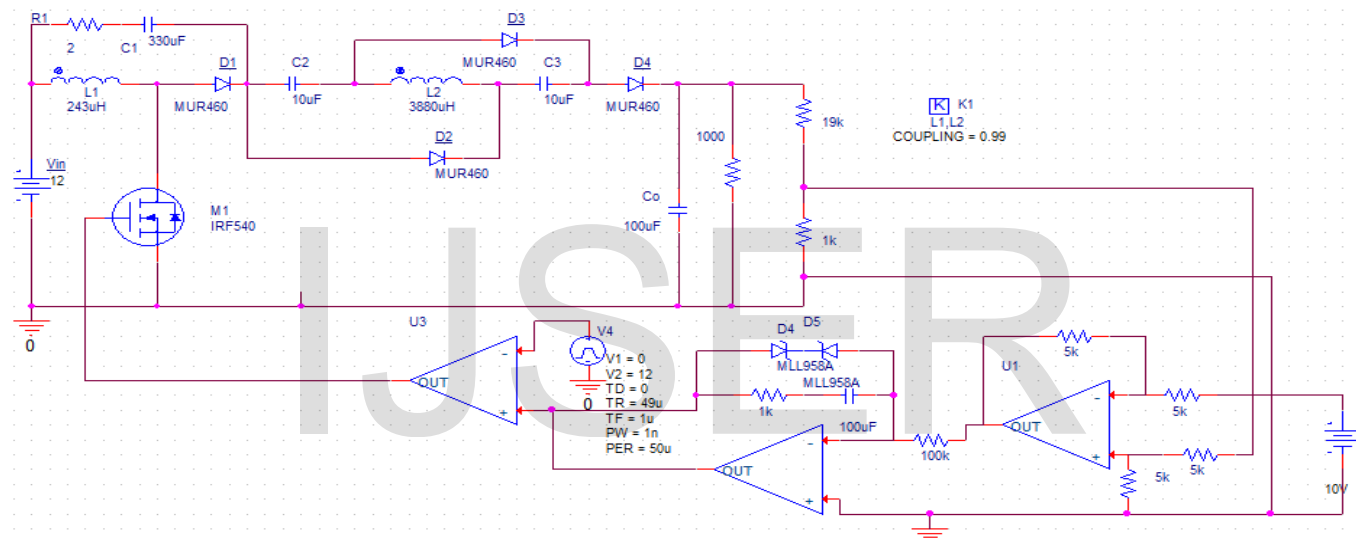


Fig. 11: Schematic of Converter with proposed control circuit.

C. Experimental Results

A hardware prototype is developed based on the above design specifications as shown in Fig. 12(f). An analog voltage mode PI controller is designed with discrete components for the closed loop operation of the converter. The functionality of converter is tested in open and closed loop operation. The steady state and transient performance of the converter are demonstrated below.

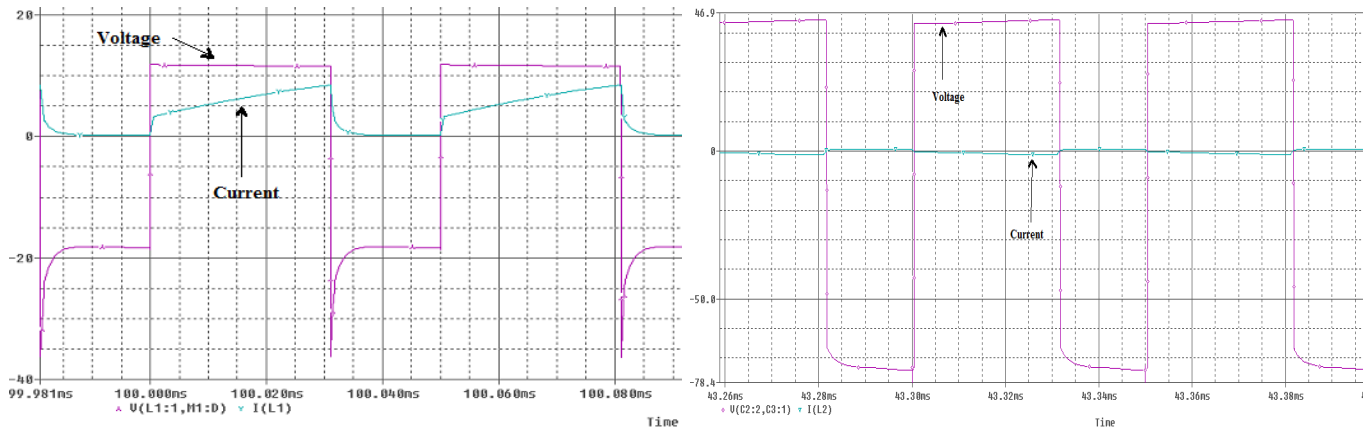
1) *Steady state performance:* The functionality of the converter under steady state has been verified for both open loop and closed loop operation under continuous conduction mode (CCM).

Fig. 13 (a) and 13 (b) show the key waveform of the voltage and current of inductors L_1 and L_2 respectively at 62% in open loop operation of the converter. The output voltage of the converter and voltage stress across switch for open loop operation of the converter is shown in Fig.13 (c). It is observed

voltage across switch is clamped by clamped capacitor (C_1) to sum of the input voltage (V_{in}) and the voltage across clamp capacitor (V_{C_1}) which is 30V.

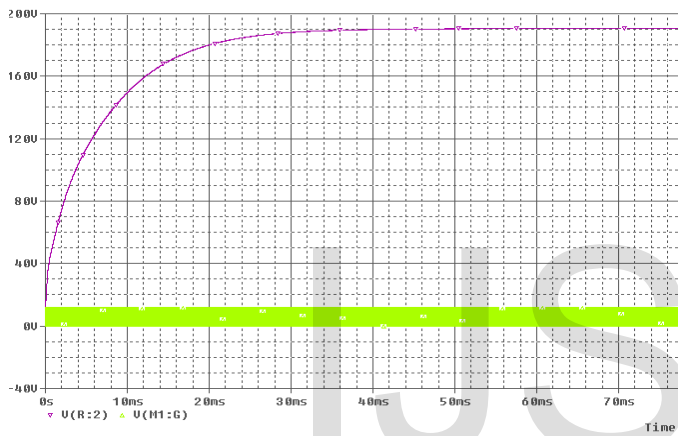
The experimental validation of the converter in steady state can be verified by Fig. 13 (e). It shows plot of output voltage v/s load current. It is observed that converter can regulate its output voltage over a wide range of variation in load (from 56% to 108% of full load).

2) *Transient performance:* The transient performance of the converter has been verified for closed loop operation under continuous conduction mode (CCM) by Fig.13 (d) and 13 (f). Fig. 13 (d) shows output voltage of the converter for different reference voltages which demonstrates that output voltage of the converter tracks the reference voltage over a wide range (from 120V to 200V). Fig. 13 (f) verifies the transient performance of the converter by regulating its output voltage when it is subjected to transient change in load (108% to 86% to 108% of full load).

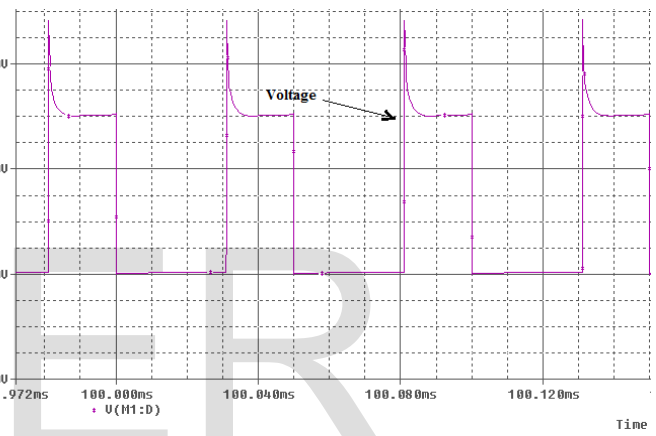


(a)

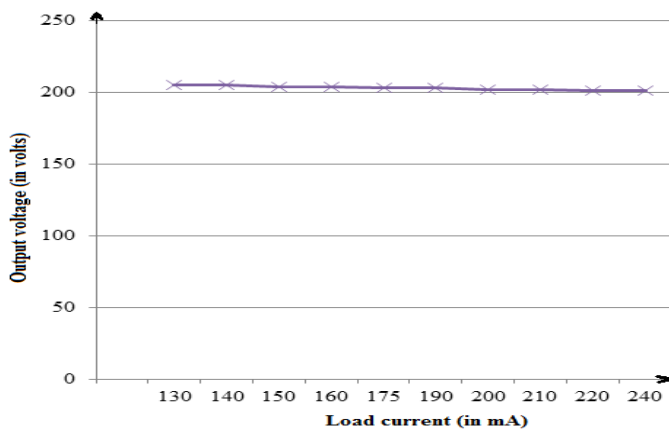
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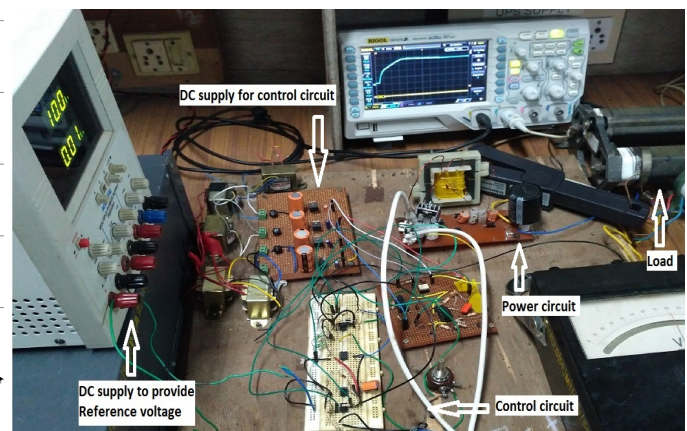
(c)



(d)

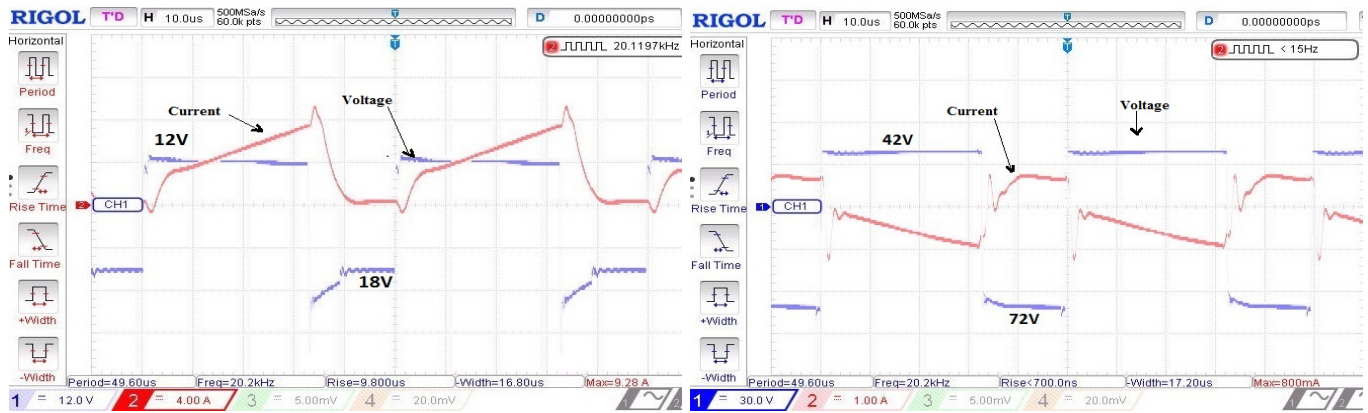


(e)



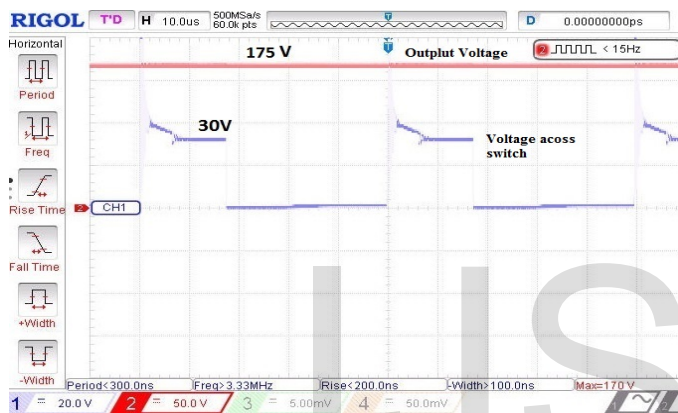
(f)

Fig. 12: Pspice simulation results: (a) Current and voltage wave forms of primary winding of coupled inductor. (b) Current and voltage wave forms of secondary winding of coupled inductor. (c) Output voltage of the converter. (d) Voltage stress across switch. (e) Load regulation plot. (f) Hardware setup.

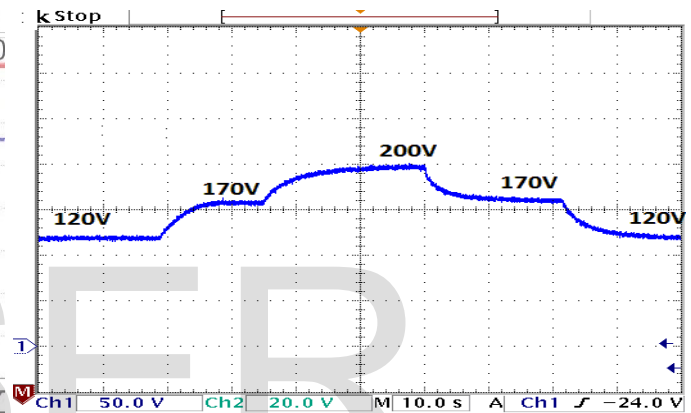


(a)

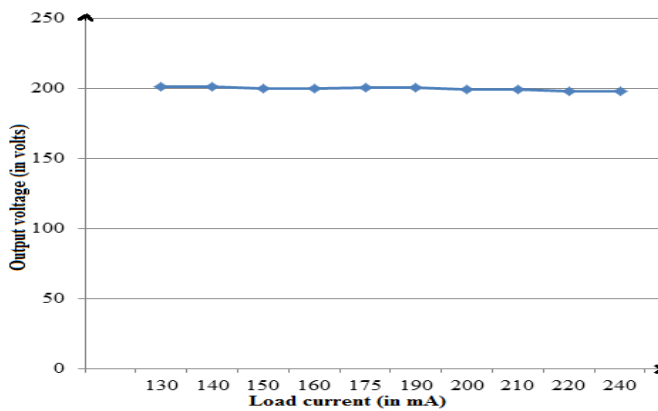
(b)



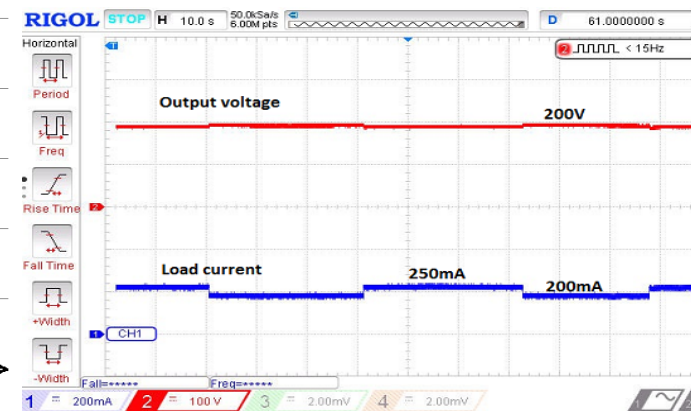
(c)



(d)



(e)



(f)

Fig. 13: Experimental results:(a) Current and voltage wave forms of primary winding of coupled inductor. (b) Current and voltage wave forms of secondary winding of coupled inductor. (c) Output voltage of the converter and Voltage stress across switch. (d) Output voltage of the converter for different values of reference voltages (V_{ref}). (e) Load regulation plot. (f) Output voltage and load current when load changes dynamically.

V. CONCLUSION

This paper presents design and implementation of a high gain dc-dc boost converter for PV systems. A simple voltage mode controller is proposed to regulate the output voltage of the converter. Functionality of the converter under both open loop and closed loop operation is validated with reference voltage and load transient operation with and experimental results. It is observed that the proposed controller can regulate the output voltage of the converter over a wide range of both reference voltage (from 120V to 200V) and load variation (56% to 108% of full load).

REFERENCES

- [1] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "A novel high step-up dc-dc converter for a microgrid system," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1127–1136, April 2011.
- [2] N. P. Papanikolaou and E. C. Tatakis, "Active voltage clamp in flyback converters operating in ccm mode under wide load variation," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 3, pp. 632–640, June 2004.
- [3] R. Watson, F. C. Lee, and G. C. Hua, "Utilization of an active-clamp circuit to achieve soft switching in flyback converters," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, Jun 1994, pp. 909–916 vol.2.
- [4] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 65–73, Jan 2003.
- [5] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless dc-dc converters with a very high dc line-to-load voltage ratio," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 3, May 2003, pp. III-435–III-438 vol.3.
- [6] R.-J. Wai and R.-Y. Duan, "High step-up converter with coupled-inductor," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1025–1035, Sept 2005.
- [7] R. J. Wai and R. Y. Duan, "High-efficiency dc/dc converter with high voltage gain," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 4, pp. 793–802, July 2005.
- [8] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc pwm converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, March 2008.
- [9] F. L. Luo and H. Ye, "Positive output super-lift converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 105–113, Jan 2003.
- [10] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor (sc)/switched inductor (sl) structures for getting hybrid step-down cuk/sepic/zeta converters," in *2006 IEEE International Symposium on Circuits and Systems*, May 2006, pp. 4 pp.5063–5066.
- [11] F. L. Luo, "Six self-lift dc-dc converters, voltage lift technique," *IEEE Transactions on Industrial Electronics*, vol. 48, no. 6, pp. 1268–1272, Dec 2001.
- [12] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched coupled-inductor cell for dc-dc converters with very large conversion ratio," in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, Nov 2006, pp. 2366–2371.
- [13] B. R. Lin and F. Y. Hsieh, "Soft-switching zeta flyback converter with a buck boost type of active clamp," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, pp. 2813–2822, Oct 2007.
- [14] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, "Boost converter with coupled inductors and buck boost type of active clamp," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 154–162, Jan 2008.
- [15] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *IEE Proceedings - Electric Power Applications*, vol. 151, no. 2, pp. 182–190, Mar 2004.
- [16] T. J. Liang and K. C. Tseng, "Analysis of integrated boost-flyback step-up converter," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 2, pp. 217–225, March 2005.
- [17] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up dc-dc converter with coupled-inductor and voltage-doubler circuits," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4196–4206, Sept 2011.
- [18] K. C. Tseng, C. C. Huang, and W. Y. Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 3047–3057, June 2013.
- [19] B. S. Revathi and M. Prabhakar, "Non isolated high gain high power dc-dc converter," in *2014 IEEE 2nd International Conference on Electrical Energy Systems (ICEES)*, Jan 2014, pp. 223–228.
- [20] J.-W. Baek, M.-H. Ryoo, T.-J. Kim, D.-W. Yoo, and J.-S. Kim, "High boost converter using voltage multiplier," in *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005.*, Nov 2005, pp. 6 pp.567–572.
- [21] B. M. Mathews and M. Barai, "A synchronized voltage-mode control for a multi-port dc-dc converter," in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2016, pp. 1–6.